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DESIGN NOTES

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LT1056 Improved JFET Op Amp Macromodel Slews Asymmetrically

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SPICE macromodels for op amps have been available for some time, for both bipolar[1,2] and JFET[3] input stage device types. Interestingly however, not much attention has been given in the models available to controlled slewing asymmetry. Dependent upon a given amplifier design topology, the large signal characteristics can have various degrees of slew rate (SR) asymmetry. It therefore makes sense to have models which emulate real IC parts in this regard.

A case in point is that of the available P-channel JFET input op amps, many which have a characteristic SR response which is asymmetrical. In fact, popular op amps with topologies like the original 355/356 types are intrinsically faster for negative going output swings than they are for positive. Similar comments apply to such related devices as the OP15, OP16, etc. Since this type of JFET device topology was introduced, the SR specified on the data sheet has typically been the **lower** of two dissimilar rates, i.e., the slower, **positive edge** SR. Thus, given an op amp with a typical SR spec of 14V/µs for positive going edges, the same amp will have a corresponding negative SR of about 28V/µs.

Ironically, this quite common JFET amplifier slewing characteristic has not been well modeled thus far. Most macromodels currently available simply do not address the asymmetric SR issue at all. Others have means of modeling it, but it is seldom found used.

A means of SR control was built into the original Boyle[1] model, and it addresses SR asymmetry for common mode (CM) signals by means of a common emitter (source) capacitor, CE (CS, for JFET amps). However, using this capacitor alone for a general SR symmetry control mechanism leaves something to be desired, as the resulting slopes are not consistent. LTC has implemented a new means of modeling SR asymmetry, shown in Figure 1.

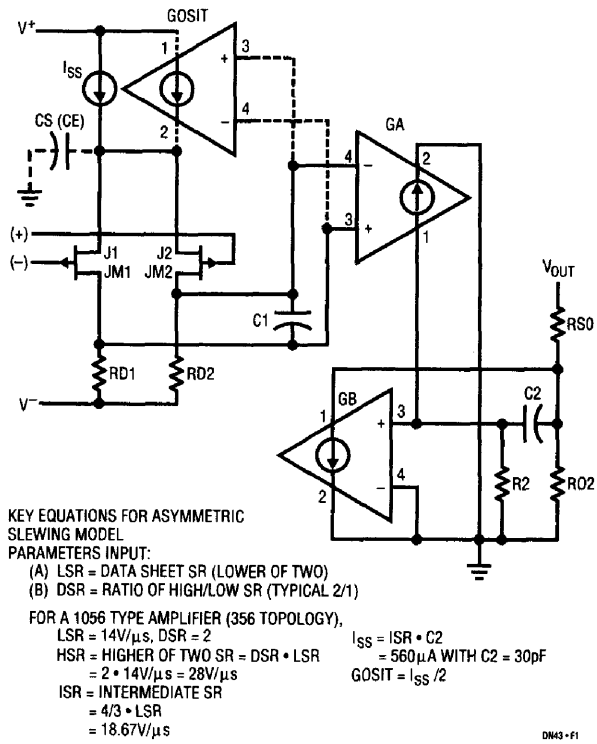

Figure 1. The LTC Asymmetric Slewing JFET Macromodel Has Little Additional Complexity, But Offers Controlled Slewing Response.

The circuit as shown here is a simplified Boyle type model with P-channel JFET input devices, J1 and J2. As this type (or similar input structure) of model is typically used, the SR is simply $I_{SS}/C2$, which is symmetrical when CS is zero. When the common source capacitor CS is added, the SR for CM signals can be adapted (corresponds to CE in the Boyle paper). Unfortunately, this strategy works best for CM amplifier inputs, and not as well for inverting inputs.

The LTC method of modeling asymmetrical SR employs an added VCCS (shown dotted), which dynamically modifies the total tail current available to J1/J2. This controlled source, "GOSIT," is driven by the differential

output of J1/J2 and produces a current which adds to or subtracts from the fixed current, I_{SS}. The resulting current available to charge/discharge compensation cap C2 is thus higher for one slewing slope than it is for the opposite. This is true regardless of whether the amplifier is operating in an inverting or non-inverting input mode. As an option, CS can still be used for further control of slewing for CM inputs (shown dotted).

In generating a new macromodel with asymmetrical SR, the **lower** of the two slew rates is input from the data sheet. Also input is the **ratio** of the high-to-low SR. Algorithms in the program used by LTC then calculate an appropriate static value for I_{SS} and the gain of VCCS GOSIT, so that the proper slewing characteristic will be produced by the model.

A representative example op amp with these characteristics is the LT1056, a high performance op amp topologically much like the LF156-LF356 and OP-16 types (also produced by LTC, with corresponding macromodels available). Some sample lines of code taken directly from the LT1056 model released in version 2.0 of the LTC library are shown below. These are shown for both the asymmetric form as released, and for an (edited) symmetric case.

Actually, only one SPICE model element is added to produce the asymmetric SR as opposed to symmetric, and that is the VCCS GOSIT. The LT1056 example below produces SR of +14V/µs and −28V/µs.

```
**
C1  80  90  1.5000E-11
ISS 7   12  5.6000E-04
GOSIT  7  12  90  80  2.8000E-04
* intermediate
```

When the controlled source GOSIT is omitted, the model reverts to simple symmetric slewing, where the SR will be $\pm(I_{SS})/C2$. This is shown below, with I_{SS} adjusted for a (symmetric) SR of 14V/µs. Those lines of code edited are shown in **bold**.

```
**
C1  80  90  1.5000E-11
* for a (symmetric) SR of 14V/µs,
* iss = (1.4e7)*(3e-11) = 420µA
ISS 7  12  4.2000E-04
* comment out gosit with first column "*"
* GOSIT 7  12  90  80  2.8000E-04
* intermediate
```

The non-inverting mode waveforms of a typical SPICE run using the LT1056 macromodel and parallel lab results with an actual LT1056 device are shown in Figures 2A and 2B, respectively. As noted, there is quite reasonable correspondence between the two. A complete LT1056 model is contained on the LTC SPICE diskette.

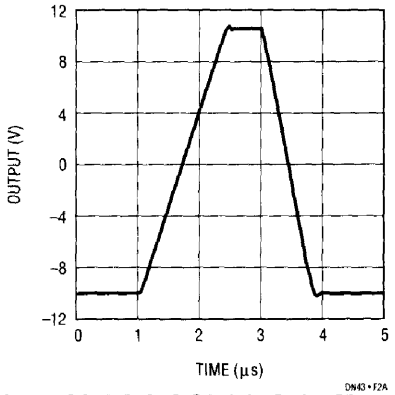

Figure 2A. LT1056 SR (+) Mode, Macromodel

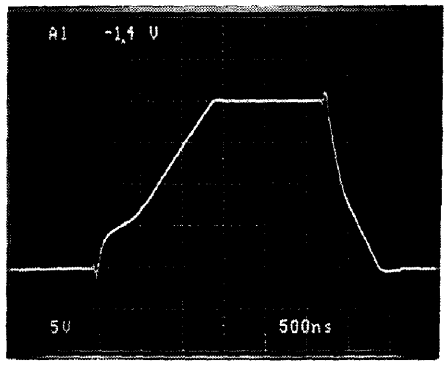

Figure 2B. LT1056 SR (+) Mode, Lab Photo

References

Available from LTC literature service, at (800) 637-5545 are copies of the latest LTC SPICE macromodel library on either a 5.25" or a 3.5" high density floppy diskette.

1. Boyle, G.R., Cohn, B.M., Pederson, D.O., Solomon, J.E., "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-9, #6, December 1974.
2. Solomon, J.E., "The Monolithic Op Amp: A Tutorial Study," *IEEE Journal of Solid-State Circuits*, Vol. SC-9, #6, December 1974.
3. Krajewska, G., Holmes, F.E., "Macromodeling of FET/Bipolar Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-14, # 6, December 1979.